

FOR ENERGY EFFICIENT INNOVATIONS

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WBG - NCP51810 Half-Bridge 150 V GaN Driver Eval Board

Public Information



NCP51810 Half Bridge 150 V GaN Driver

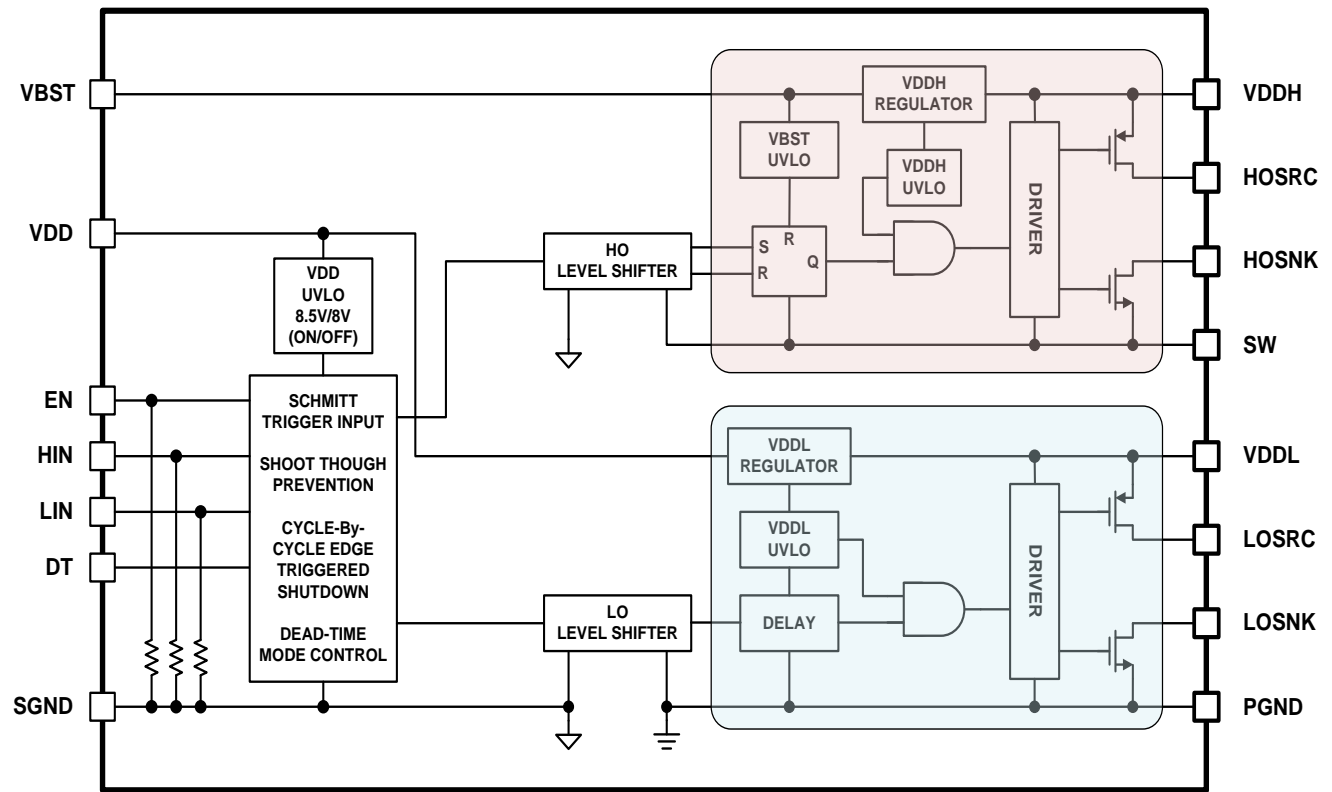
Features and Benefits

- 150 V, Integrated High-Side and Low-Side Gate Drivers
- Independent UVLO for VDD, High and Low-Side Drive Regulators
- Typical 1 A/2 A Source/Sink Current
- Separate Source/Sink Driver Output Pins
- 5.2 V Regulated Drive Optimized for GaN
- 1 ns Rise and Fall Times
- 200V/ns dV/dt Immunity
- Max Propagation Delay of 50 ns
- Programmable Dead-time
- QFN 4mm x 4mm 15 Leads

Applications

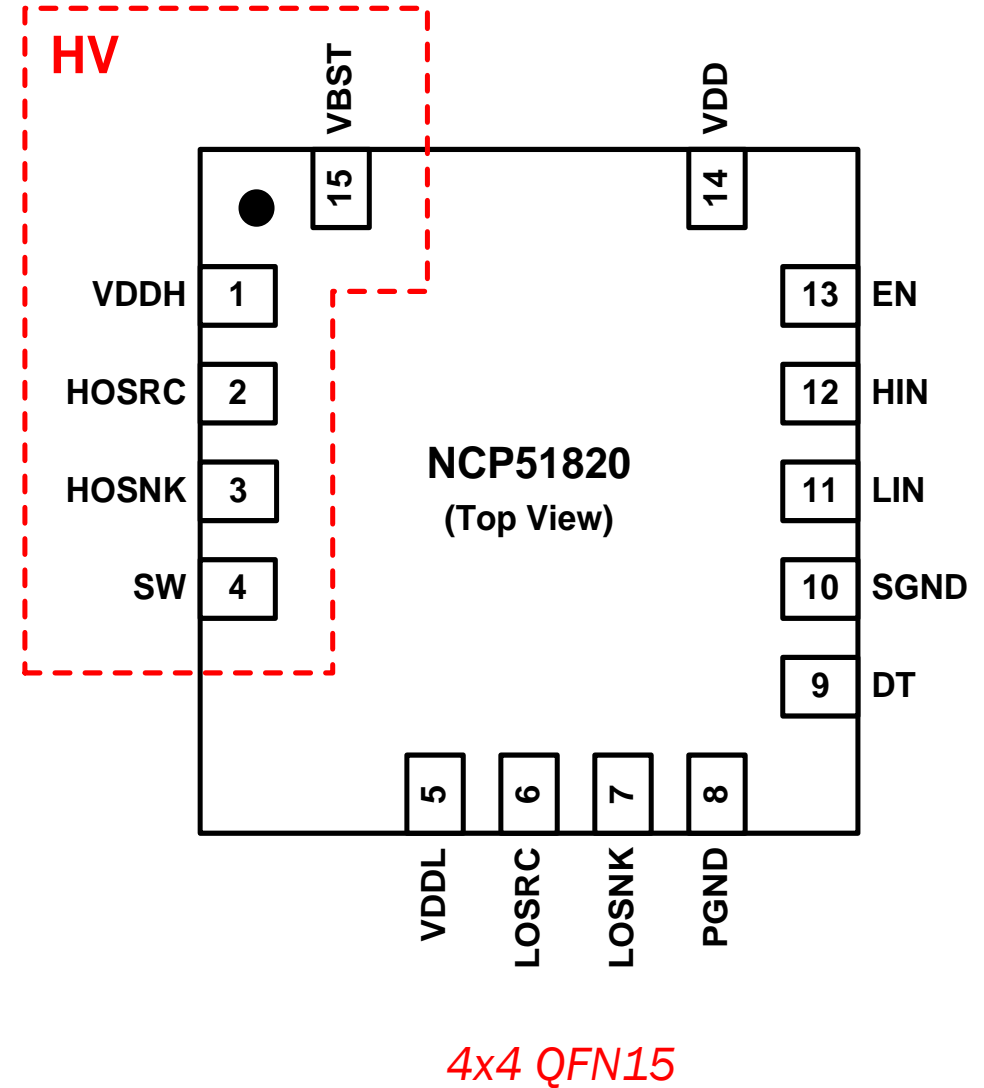
- Datacenter 48 V → 12 V Bricks and Board POL
- Telecom
- Industrial Power Module

Block Diagram

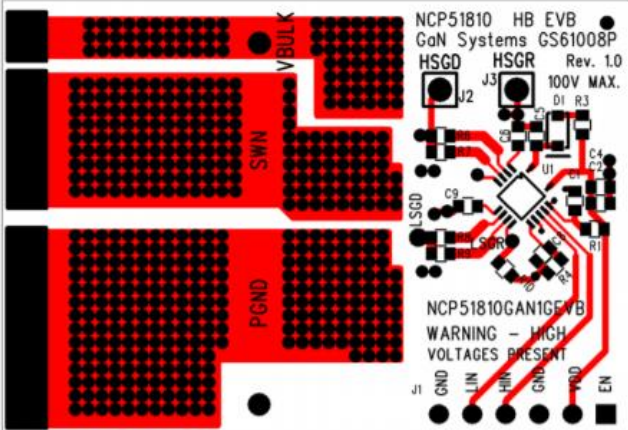


NCP51810 Pin Descriptions

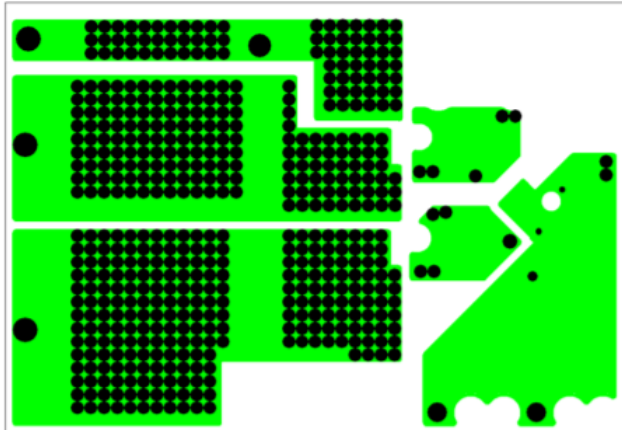
1. **VDDH** – local bias rail for the high-side driver
2. **HOSRC** – high-side driver source output
3. **HOSNK** – high-side driver sink output
4. **SW** – switch-node (high-side GaN source return)
5. **VDDL** – local bias rail for the low-side driver
6. **LOSRC** – low-side driver source output
7. **LOSNK** – low-side driver sink output
8. **PGND** – power ground (low-side GaN source return)
9. **DT** – dead-time adjust (mode select)
10. **SGND** – signal ground (reference for all logic control signals)
11. **LIN** – TTL input logic signal for the low-side driver
12. **HIN** – TTL input logic signal for the high-side driver
13. **EN** – TTL enable signal for the driver (active HIGH)
14. **VDD** – IC bias supply voltage rail (8 V – 20 V)
15. **VBST** – bootstrap positive bias voltage



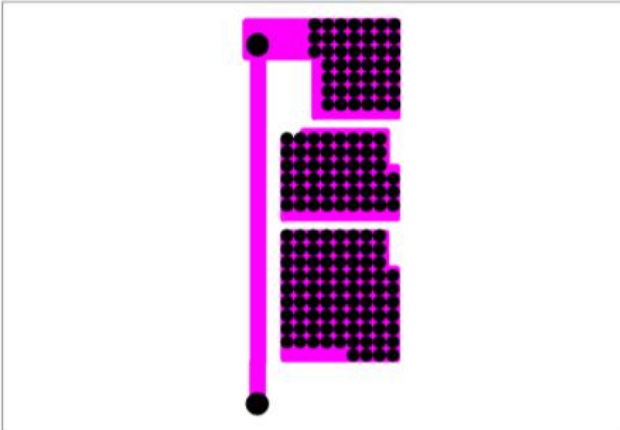
NCP51810 + 100 V GaNFET Mini EVB: Four Layer PCB



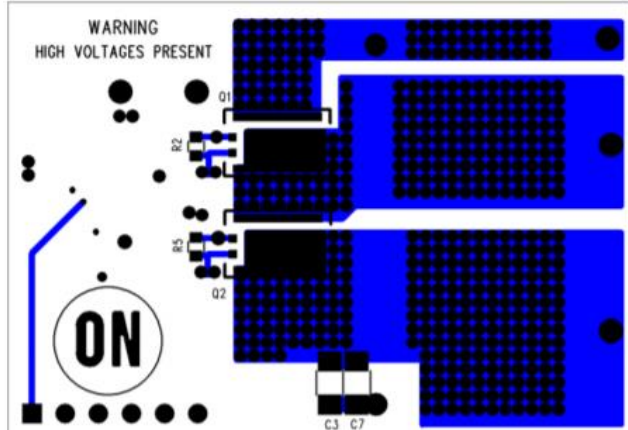
Layer 1



Layer 2

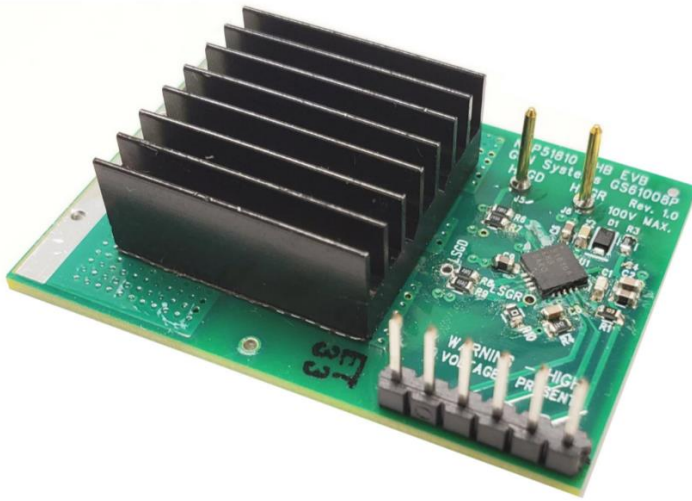


Layer 3

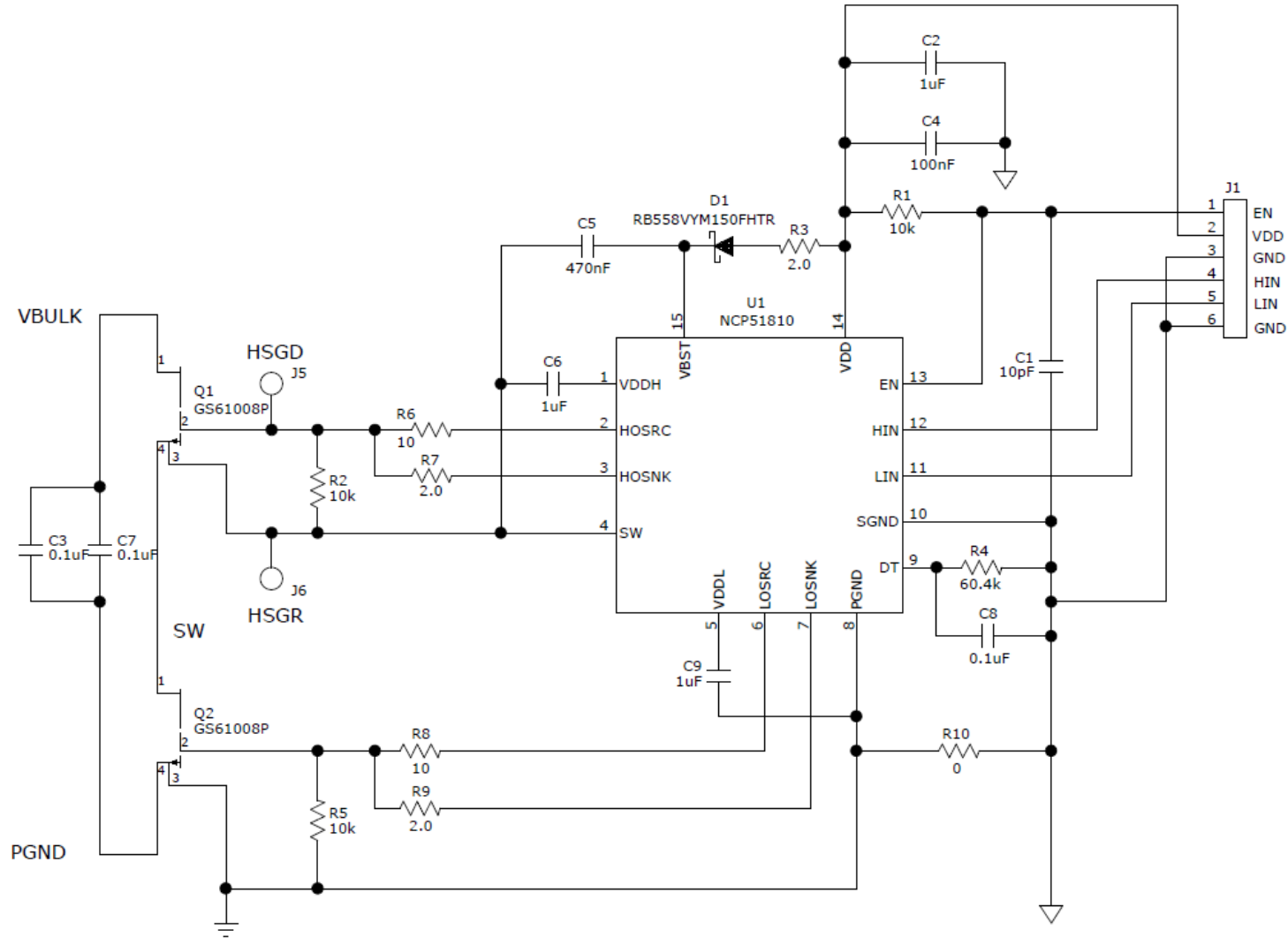


Layer 4

- 100 V GaNFET EVB shown
 - Shown with heatsink (orderable without heatsink)
 - For high-power applications, customer needs to provide their own heatsink and/or fan cooling



NCP51810 Mini EVB: Schematic



Please refer to
EVBUM2762 on
www.onsemi.com
for EVB userguide

